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Substitute for form 1449A/PTO		<b>Complete if Known</b>	
<b>INFORMATION DISCLOSURE STATEMENT BY APPLICANT</b>		Application Number: 10/755,042	
		Filing Date: January 9, 2004	
		First Named Inventor: <b>MOU-SHIUNG LIN</b>	
		Art Unit: 2815	
		Examiner Name: <b>JEROME JACKSON, JR.</b>	
(Use as many sheets as necessary)			
Sheet	1	of	3
Attorney Docket No: 085027-0104			

US PATENT DOCUMENTS					
Examiner Initial *	Cite No	Document Number	Publication Date	Name of Patentee or Applicant of Cited Document	Pages, Columns, Lines, Where Relevant Passages or Relevant Figures Appear
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FOREIGN PATENT DOCUMENTS						
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		NONE				

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Examiner Initials*	Cite No <sup>1</sup>	Include name of the author (in CAPITAL LETTERS), title of the article (when appropriate), title of the item (book, magazine, journal, serial, symposium, catalog, etc.), date, page(s), volume-issue number(s), publisher, city and/or country where published.			T <sup>2</sup>
	1	MISTRY, K. et al. "A 45nm Logic Technology with High-k+ Metal Gate Transistors, Strained Silicon, 9 Cu Interconnect Layers, 193nm Dry Patterning, and 100% Pb-free Packaging," IEEE International Electron Devices Meeting (2007) pgs. 247-250			
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	10	EDELSTEIN, D. et al. "Full Copper Wiring in a Sub-0.25 pm CMOS ULSI Technology," Technical Digest IEEE International Electron Devices Meeting (1997) pgs. 773-776	
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